

INFORMATION DISCLOSURE STATEMENT PURSUANT TO
37 C.F.R. §§1.97-1.99

PATENT APPLICATION

Applicant(s): Krishnendu Mondal *et al.*

Docket No.: END920030091US1

FOR: MULTIPLE ON-CHIP TEST RUNS AND REPAIRS FOR MEMORIES

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure under 37 C.F.R. §1.56 and pursuant to 37 C.F.R. §§1.97-1.99, Applicant(s) hereby notifies the U.S. Patent and Trademark Office of the documents listed on the attached Form PTO-1449. Applicant respectfully submits that all pending claims are patentable over the foregoing references, alone or in combination. The Examiner is requested to initial the enclosed Form PTO-1449 and return a copy thereof to the undersigned.

The submission of the listed documents is not intended as an admission that any such document constitutes prior art against the claims of the present application. Applicant reserves the right to dispute any of the listed documents as prior art during examination. Further, Applicant does not waive any right to take any action that would be appropriate to antedate or otherwise remove any listed document as a competent reference against the claims of the present application. Furthermore, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made or that no other material information may exist. This Information Disclosure Statement is being filed within three months of the filing date of the captioned patent application, and therefore no certification under 37 C.F.R. §1.97(e) or fee under 37 C.F.R. §1.17(p) is required.

Respectfully submitted,

Dated: 10/31/2003.

By Jack P. Friedman
Jack P. Friedman
Reg. No. 44,688

Enclosures: PTO-1449

INFORMATION DISCLOSURE CITATION*(Use several sheets if necessary)*

ATTY DOCKET NO.

END920030091US1

SERIAL NO.

Krishnendu Mondal et al.

FILING

GROUP

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6,574,757	6/2003	Park et al.			
	6,560,740	5/2003	Zuraski, Jr. et al.			
	6,505,324	1/2003	Cowan et al.			
	6,469,949	10/2002	Hsu et al.			
	6,408,401	6/2002	Bhavsar et al.			
	6,405,331	6/2002	Chien			
	6,367,042	4/2002	Phan et al.			
	6,182,257	1/2001	Gillingham			
	6,141,267	10/2000	Kirihata et al.			
	6,073,258	6/2000	Wheater			
	5,841,784	11/1998	Chan et al.			

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		Barth et al., METHOD TO REDUCE CHIP YIELD LOSS DUE TO FUSES INCORRECTLY BLOWN, Research Disclosure, May 1990, Number 313, 1 page.
		IBM Technical Disclosure Bulletin R. J. Prilik, Vol. 30, No. 11, April 1988, REPAIR CALCULATION FOR RANDOM-ACCESS MEMORY REDUNDANCY USING BUILT-IN LOGIC AND SCANNABLE LATCHES, pages 424-425.

EXAMINER

DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5,805,789	9/1998	Huott et al.			
	5,764,878	6/1998	Kablanian et al.			
	5,659,551	8/1997	Huott et al.			

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